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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,292	PATEL ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-21,26-30,65-85 and 87-107* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *65-85 and 87-107* is/are allowed.

6)☒ Claim(s) *16-21 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed June 04, 2004 (Certificate of Mailing date: June 01, 2004). The Examiner acknowledges the amendments to the Specification and Claims, the cancellation of Claims 22-25 and 86 and the addition of new Claims 100-107. Accordingly, Claims 16-21, 26-30, 65-85 and 87-107 are now pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Mosley (US 2002/0071258 A1) Naito et al. (US 6,556,420 B1)

Salem (US 6,300,677 B1)* Patel et al. (US 5,929,646)

*Already of record in the instant Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 16-21 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Salem.

As to Claim 16, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a substantially planar upper surface (i.e., the upper surface of substrate 84 to which IC 82 is mounted) and a plurality of conductors (not shown, but on the upper surface of substrate 84 for electrically connecting the IC 82; Fig. 4A and col.4: 14-17) within an IC mounting region on the upper surface of substrate 84; at least one capacitor 86 within the IC mounting region ("within" in the sense of --*surrounded by*--, or, --*within the mounting region perimeter defined by the bumps of the IC 82 mounted on*-- the IC mounting region of the upper surface of substrate 84; Figs. 4A and 4B), wherein the at least one capacitor 86 comprises top and bottom surfaces 54 and 56, respectively, each having a plurality of terminals 42, 44, 46 and 48 of first and second polarity types (col.2: 58-62; col.3: 9-15 and 46-57), wherein a selected terminal 42 of first polarity type (positive; col.3: 46-57) on the bottom surface 56 (col.2: 58-67) is electrically coupled to a first conductor (on the surface of conductive well 88; Fig. 4A and col.4: 12-17 and 24-26) and wherein a selected terminal 44 of second polarity type (negative; col.3: 46-57) on the bottom surface 56 (col.2: 58-67) is electrically coupled to a second conductor (on the surface of conductive well 88; Fig. 4A and col.4: 12-17and 24-26); an IC 82 comprising a plurality of terminals (bumps) on a surface thereof (Fig. 4A; col.4: 12-17), wherein the IC (bump) terminals are electrically coupled to selected terminals of first and second polarity types on the top surface 54 of capacitor 86 (col.3: 40-57 and col.4: 12-13).

As to Claim 17, Salem further discloses the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with

the structure of at least one capacitor 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to the capacitor 86).

As to Claim 18, Salem further discloses the at least one capacitor 86 is mounted atop the first and second conductors on the surface of conductive well 88 (Fig. 4A; col.4: 24-26).

As to Claim 19, Salem further discloses the at least one capacitor 86 is mounted atop three conductors; i.e., the conductors in the conductive well 88 that receive terminals 42, 44, 46 and 48 of each capacitor 86 (Figs. 2 and 4A; col.3: 40-65 and col.4: 24-26).

As to Claim 20, Salem further discloses that the at least one capacitor 86 in Fig. 4A (40 in Fig. 2) is a capacitor array (Fig. 2; col.3: 8-15 and 44-57).

As to Claim 21, Salem further discloses the plurality of terminals are disposed over substantially the entire top and bottom surfaces 54 and 56, respectively (sections 42, 44, 46 and 48 are each metal sections and top portions 54, bottom portions 56 and the side portions are all continuous metal terminals with sites 50 and 52 for surface mount bump connections; Fig. 2 and col.2: 58-col.3: 15).

As to Claim 26, Salem further discloses the **plurality of conductors** (on the **upper** surface of package substrate 84) are substantially parallel to one another (this is inherently so due to the disclosed terminal configuration of the IC 82 and the assembly of capacitor arrays 86 wherein the terminal configuration of the plurality of conductors is that of parallel linear arrays (Figs. 4A,B,C).

As to Claim 27, Salem further discloses the at least one capacitor 86 is **non-orthogonally mounted** atop the **first** and **second** conductors (in conductive well 88) to which it is electrically coupled; i.e., capacitor 86 is mounted such that it lies parallel (i.e., non-orthogonal) to the **first** and **second** conductors in conductive well 88 of package substrate 84.

As to Claim 28, Salem further discloses a plurality of capacitors 86 distributed substantially throughout the IC mounting region, each capacitor 86 being in electrical contact with at least one of the conductors of substrate 84.

As to Claim 29, Salem further discloses the plurality of capacitors 86 comprises a plurality of sets of capacitors: For example, capacitor 86 is a larger embodiment of similar capacitor 40 (col.3: 10-15), wherein capacitor 40 comprises a set of two capacitors, the first capacitor formed of metal sections 42, 44 and the second capacitor formed of metal sections 46, 48. There are a plurality of such capacitors 86 that each are formed of a set of four capacitors--each formed of two metal sections just like capacitor 40--as shown in Fig. 4C. Each capacitor set 86 comprising the four capacitors aligned substantially end-to-end (compare Figs. 2 and 4C).

5. Claims 16-21, 26, 27 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Mosley.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to Claim 16, Mosley discloses, in Figs. 1A, 1B and 2: a substrate 209 having a substantially planar upper surface and a plurality of conductors 218 within an IC mounting region on the upper surface (substrate 206 being the IC; lines 4-6 of paragraph [0022], lines 1-6); at least **one** capacitor 100 within the IC mounting region, wherein the at least one capacitor comprises top and bottom surfaces 127 and 130, respectively, each having a plurality of terminals 133 (paragraph [0018], lines 19-22) of first and second polarity types (i.e., the first polarity type corresponding to a high voltage site 139 of terminals 133 and the second polarity type corresponding to a low voltage site 142, 145, 148 and 151 of terminals 133; Figs. 1A, 1B and paragraph [0020]), wherein a selected terminal of first polarity type on the bottom surface 130 (due to plated through-holes electrically connecting top and bottom terminals 133; paragraph [0018], lines 19-22) is electrically coupled to a first conductor 218 on substrate 209 (Fig. 2), and wherein a selected terminal of second polarity type on the bottom surface 130 (due to plated through-holes electrically connecting the top and bottom terminals 133; paragraph [0018], lines 19-22) is electrically coupled to a second conductor 218 on substrate 209 (Fig. 2); and an IC 206 (paragraph [0022], lines 1-6) comprising a plurality of IC terminals 215 on a surface thereof, wherein the IC terminals are electrically coupled to selected terminals of first and second polarity types on the top surface 127 of capacitor 100 (Figs. 1B and 2; paragraphs [0020] and lines 9-15 of [0022]).

As to Claim 17, Mosley further discloses the first conductor 218 is to couple to a first potential (e.g., by coupling to the high voltage terminal 139 of terminals 133; Figs. 1B and 2; paragraph [0020]), and the second conductor 218 is to couple to a second potential (e.g., by coupling to the low voltage terminal 142; Figs. 1B and 2; paragraph [0020]).

As to Claim 18, Mosley further discloses the at least one capacitor 100 is mounted atop the first and second conductors 218 (Fig. 2).

As to Claim 19, Mosley further discloses the at least one capacitor 100 is mounted atop at least three conductors 218 (Fig. 2).

As to Claim 20, Mosley further discloses, in Fig. 1A, that the at least one capacitor 100 is a capacitor array (i.e., a capacitor comprising at least one surface having more than one terminal of a given polarity type; e.g., terminals 133 arranged as terminals 139, 142, 145, 148 and 151 throughout the upper and lower surfaces of capacitor 100, as disclosed in Fig. 1B and paragraph [0020]).

As to Claim 21, Mosley further discloses the plurality of capacitor terminals 133 are disposed over substantially the entire top and bottom surfaces of capacitor 100 (Figs. 1A and 1B).

As to Claim 26, Mosley further discloses the plurality of conductors 218 on substrate 209 are arranged in an array corresponding to the array of terminals 133 of capacitor 100 which are arranged substantially parallel to one another (i.e., the plurality of conductors 218 of substrate 209 are arranged as parallel linear arrays corresponding

to the parallel linear array arrangement of the capacitor terminals 133; Figs. 1B and 2; lines 9-11 of paragraph [0022]).

As to Claim 27, Mosley further discloses the at least one capacitor 100 is **non-orthogonally mounted** atop the **first** and **second** conductors 218 of substrate 209 to which it is electrically coupled; i.e., capacitor 100 is mounted such that it lies parallel (i.e., non-orthogonal) to the **first** and **second** conductors 218 of substrate 209 (Fig. 2).

As to Claim 30, Mosley further discloses the conductors 218 include pads (i.e., the conductive sites on substrate 209 to which solder bumps 215 are mounted; Fig. 2; paragraph [0022], lines 9-11).

6. Claims 16-21, 26, 27 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Naito et al.

As to Claim 16, Naito et al. discloses: a substrate 62b having a substantially planar upper surface 63 and a plurality of conductors (i.e., the conductors on surface 63 that receive the surface-mounted IC 64) within an IC mounting region on upper surface 63 (Fig. 2); at least one capacitor 41a (Fig. 5) [41b in Fig. 7] within the IC mounting region (i.e., "within" in the sense of the capacitor 41b being mounted to the substrate beneath, and directly connected to, the pads of the IC mounting region by means of the substrate through-vias, as shown in Fig. 7); wherein the at least one capacitor comprises top and bottom surfaces 48 and 50, respectively, (Fig. 5) each having a plurality of terminals 49a, 51a, 49b and 51b of first and second polarity types (Figs. 5 and 7; col.8: 51-59; col.9: 1-13 and 43-56), wherein a selected terminal 51b of first polarity type on the bottom surface is electrically coupled to a first conductor (the first

conductor being on the surface of circuit board 67; col.9: 10-13), and wherein a selected terminal 49b of second polarity type on the bottom surface 50 is electrically coupled to a second conductor (the second conductor being on the surface of circuit board 67; col.10: 13-16 [Examiner's Note: as shown in Figs. 5 and 7, and indicated in col.9: 53-56, "49a" in col.10: 13-16 is incorrect and should be read as --49b--]); and an IC 64 (Fig. 7 and col.8: 27-30) comprising a plurality of IC terminals 77 on a surface thereof (Fig. 7), wherein the IC terminals are electrically coupled to selected terminals of first and second polarity types 51a and 49a, respectively, on the surface of the capacitor 41a (Fig. 5) [41b in Fig. 7].

As to Claim 17, Naito et al. further discloses the first conductor (on the surface of circuit board 67) is to couple to a first potential (i.e., power) and the second conductor is to couple to a second potential (i.e., ground) [Fig. 7; col.9: 7-13; col.10: 13-16 and 36-45].

As to Claim 18, Naito et al. further discloses the at least one capacitor 41a (Fig. 5) [41b in Fig. 7] is mounted atop the first and second conductors of circuit board 67 (Fig. 7; col.9; 7-13 and col.10: 13-16).

As to Claim 19, Naito et al. further discloses the at last one capacitor is mounted atop at least three conductors on circuit board 67 (Fig. 7).

As to Claim 20, Naito et al. further discloses that the at least one capacitor 41a (Fig. 5) [41b in Fig. 7] is a capacitor array (i.e., a capacitor comprising at least one surface having more than one terminal of a given polarity type; namely, ground and power; col.9: 7-13; col.10: 13-16 and 36-45).

As to Claim 21, Naito et al. further discloses the plurality of capacitor terminals 49a, 51a, 49b and 51b are disposed over substantially the entire top and bottom surfaces (Figs 1, 2 and 5; col.9: 42-56).

As to Claim 26, Naito et al. further discloses the **plurality of conductors** (on the **upper** surface 63 of substrate 62b) are substantially parallel to one another (this is inherently so due to the disclosed parallel linear array configuration of the terminals 72 of IC 64 and the corresponding parallel linear array of capacitor terminals 49a,b, 51a,b (Figs. 1, 2, 5 and 7; col.10: 36-40).

As to Claim 27, Naito et al. further discloses the at least one capacitor 86 is **non-orthogonally mounted** atop the **first** and **second** conductors (on circuit board 67) to which it is electrically coupled; i.e., capacitor 41b is mounted such that it lies parallel (i.e., non-orthogonal) to the **first** and **second** conductors on circuit board 67 (Fig. 7).

As to Claim 30, Naito et al. further discloses the conductors include pads, i.e., the conductive lands on circuit board 67 (col.9: 10-13 and col.10: 13-16).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salem in view of Patel et al.

Salem discloses the surface mounting of IC 82 and capacitors 86 on substrate 84 (col.4: 24-30) but does not explicitly depict or describe the substrate conductors that receive the IC and capacitor solder bumps and thereby effectively surface mount and electrically couple the IC 82 and capacitors 86 to the substrate 84. However, the use of pads for receiving the solder bumps of devices and thereby providing electrical connectivity between devices, and between devices and substrates, is notorious in the art of surface mounting components, as evidenced by Patel et al. (Fig. 2 and col.4: 11-14 and 55-58, wherein solder bumps 207 of module package 204 are mounted on pads 110 of substrate 100 and solder bumps 206 of module 202 are mounted on pads 104 of substrate 100; similarly in Fig. 3 and col.5: 41-54, wherein solder bumps 206 of module 202 are mounted on pads 110 of substrate 100 and solder bumps 207 and 208 of interposer 204 are mounted on substrates 100 and 300, respectively) and would have been obvious to one ordinary skill in the art at the time the invention was made for the

purpose of effecting a mechanically and electrically reliable connection of the components to the substrate, as taught in Patel et al.

Allowable Subject Matter

10. Claims 65-85 and 87-107 have been allowed.

Response to Arguments

11. Applicant's arguments and amendments of the claims in the instant Amendment, filed June 04, 2004, have placed independent Claims 65, 70, 75, 81, 100 and 105 in condition for allowance. Applicant's arguments and amendment to Claim 16 have overcome the 35 USC § 102 rejections over Drake et al., Menzies, Jr. et al., Wallace and Tao et al. set forth in the previous Office Action of March 29, 2004.

12. Applicant's arguments on pp.21-22 of the instant Amendment, filed June 04, 2004, regarding amended Claim 16 with respect to the 35 USC § 102(e) rejection over Salem (US 6,300,677 B1) have been fully considered but they are not persuasive.

(a) The Applicant argues, on p.21, that "Salem fails to disclose an IC package with a substrate having a substantially planar upper surface, because Salem's package substrate 84 contains a connection well in the upper surface." The Examiner takes issue with this interpretation of "a planar upper surface." The fact that package substrate 84 contains a well 88 is not sufficient basis to conclude that the well 88 is of a piece with the upper surface or that the well 88 is "in the upper surface;" rather, the Examiner considers the upper surface of the package substrate 84 to be the recited "**a**

substantially planar upper surface" having the "plurality of conductors within an IC mounting region on the upper surface" (bold and underlined emphasis added). Accordingly, yet *another* (say, *lower*) surface of package substrate 84 is the surface in well 88 to which the capacitors 86 are electro-mechanically coupled. It cannot be disputed that the "upper surface" of package substrate 84, so defined, is "**a substantially planar** upper surface" (bold and underlined emphasis added). There is no requirement in Claim 16 for "a substantially planar upper surface" to define the *entire and unbroken* upper surface of the package substrate 84; i.e., a smooth surface with no holes, cavities, wells or recesses, as the Applicant suggests on p.21 of the instant Amendment arguments. Therefore, the Examiner considers the recitation Claim 16 of "**a** substantially **planar upper** surface" (bold and underlined emphasis added) of package substrate 84 to be the surface to which the outer bumps of IC 82 are electro-mechanically coupled in Fig. 4A of Salem.

(b) The Applicant argues, on p.21, that "Salem fails to disclose first and second conductors **on a substantially planar upper surface** to which selected terminals of the capacitor are electrically coupled" (bold emphasis added). While it is true that the claimed first and second conductors, to which selected terminals of the capacitor are electrically coupled, are not on the substantially planar surface upper surface of the package substrate 88 of Salem, nevertheless, the above-cited structure is **not what is claimed** in Claim 16. A careful reading of Claim 16 reveals therein that selected terminals of the first and second polarity types are electrically coupled to "**a** first conductor" and "**a** second conductor," respectively (bold and underlined emphasis

added). There is no requirement recited in the claim for the "first conductor" and the "second conductor" to be "on [the] substantially planar upper surface;" i.e., there is no antecedent connection established between the recitation of "a first conductor" (line 7 of Claim 16) and the "plurality of conductors...on the upper surface" (lines 2-3 of Claim 16), and no antecedent connection established between the recitation of "a second conductor" (line 8 of Claim 16) and the "plurality of conductors...on the upper surface" (lines 2-3 of Claim 16). Therefore, the first conductors and second conductors in the connection well 88 of Salem read on "a first conductor" and "a second conductor" recited in lines 7 and 8 of amended Claim 16.

(c) Naito et al. (US 6,556,420 B1) reads on Claim 16, as indicated in the rejection set forth in the present Office Action, and also happens to teach "a substantially planar upper surface" that occupies the *entire* top surface 63 of substrate package 62b (Fig. 7).

(d) Mosley (US 2002/0071258 A1) reads on Claim 16 *exactly* as the Applicant contemplates the invention when the limitations of Claim 16 are considered in conjunction with the further structural details presented by the Applicant in the above-discussed arguments on p.21 of the instant Amendment.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
August 17, 2004